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Date: August 9, 2001

Attorney Docket No. ASA-1018



24956
PATENT TRADEMARK OFFICE

To: Assistant Commissioner for Patents
Washington, D.C. 20231

Sir: Transmitted herewith for filing is the patent application of:

Inventor: T. KATO et al (see attached)

For:

SEMICONDUCTOR INTEGRATED CIRCUIT HAVING RECEIVING AND
TRANSMITTING UNITS FORMED ON A SINGLE SEMICONDUCTOR CHIP WITH
A TEST SIGNAL INPUT PORT

Enclosed are:



4 Sheets of Drawings



This application is being filed without an executed Declaration.



Priority is claimed from Japanese Application No. 2000-242618
filed August 10, 2000. A certified copy is attached herewith.



Copies of the disclosure documents listed on the attached PTO 1449 form and
 discussed in the specification or attached Information Disclosure Statement.



A verified statement to establish small entity status under 37 CFR 1.9 and 1.27.



Specification: Abstract , Description 21 pages; and 7 claim(s).



Preliminary Amendment.



Executed Declaration.

The filing fee is calculated as shown below:

Small Entity

Large Entity

For:	No. Filed	No. Extra
Basic Fee		
Total Claims	7 -20 = * 0	
Indep Claims	4 - 3 = * 1	
<input type="checkbox"/> Multiple Dependent Claim (s)		

* If difference is less than zero
then enter '0' in second column

Rate	Fee
	\$ 355
x 9	\$
x 40	\$
+ 135	\$
Total	\$

Rate	Fee
	\$ 710
x 18	\$ 0
x 80	\$ 80
+ 270	\$ 0
Total	\$ 790



A check in the amount of \$ 790.00 is enclosed for the filing fee.



The Commissioner is hereby authorized to charge any additional fees that may be required to
Deposit Account No. 50-1417.

Respectfully Submitted,

By: 
John R. Mattingly
Registration No. 30,293

LIST OF INVENTORS' NAMES AND ADDRESSES

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